

# **RPG –XFFTS**

## **eXtended bandwidth Fast Fourier Transform Spectrometer**

**Technical Specification**

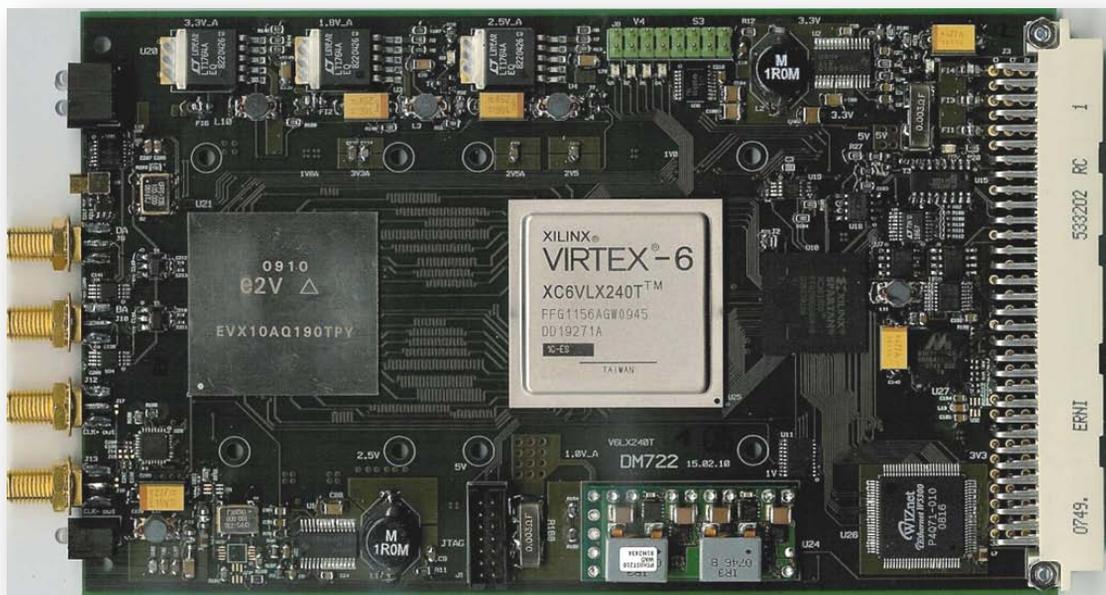


19" XFFTS crate equipped with eight XFFTS boards and one XFFTS controller

## Fast Fourier Transform Spectrometer

The RPG eXtended bandwidth **F**ast **F**ourier **T**ransform **S**pectrometer (**XFFTS**) is optimized for a wide range of radio astronomical applications. The new digitizer and analyzer boards make use of the latest versions of GHz analogue-to-digital converters (ADC) and the most complex field programmable gate array (FPGA) chips commercially available today. These state-of-the-art chips made it possible to build a digital spectrometer with instantaneous bandwidth of 2.5 GHz and 32768 (32K) spectral channels.

The XFFTS is capable of digitizing a baseband mixed intermediate frequency (IF) signal of a heterodyne receiver and transforming this digital data stream into a power spectrum in real time.



Digitizer- / Analyzer Board (XFFTS-Board)

Each XFFTS-board operates from a single 5 Volt source and dissipates less than 30 Watt, depending on the actual configuration in terms of bandwidth and number of spectral channels. Precise time stamping of the processed spectra is realized by an on-board GPS/IRIG-B time decoder. Furthermore, the 10-layer boards include a programmable ADC clock synthesizer for a wide range of configurations (bandwidth: 0.1 – 2.5 GHz), making the spectrometer flexible for different observation requirements .

The XFFTS-boards include a standard 100 MBit/s Ethernet interface, which simplifies the combination of many boards into an Array-XFFTS, simply by integration of a common buffered Ethernet switch. Up to eight XFFTS-boards can be housed in one XFFTS-crate together with power supplies (4 × 5 Volt / 20 Amperes) and one XFFTS-controller.

The XFFTS-controller manages the synchronization of the XFFTS-boards. It provides a reference clock for the on-board ADC synthesizers or the GPS/IRIG-B timing information. In addition, the XFFTS-controller displays house-keeping information on a four line LCD, like board IP numbers, temperatures of the ADC and FPGA chips as well as the power level of the IF inputs.

## TECHNICAL DATA

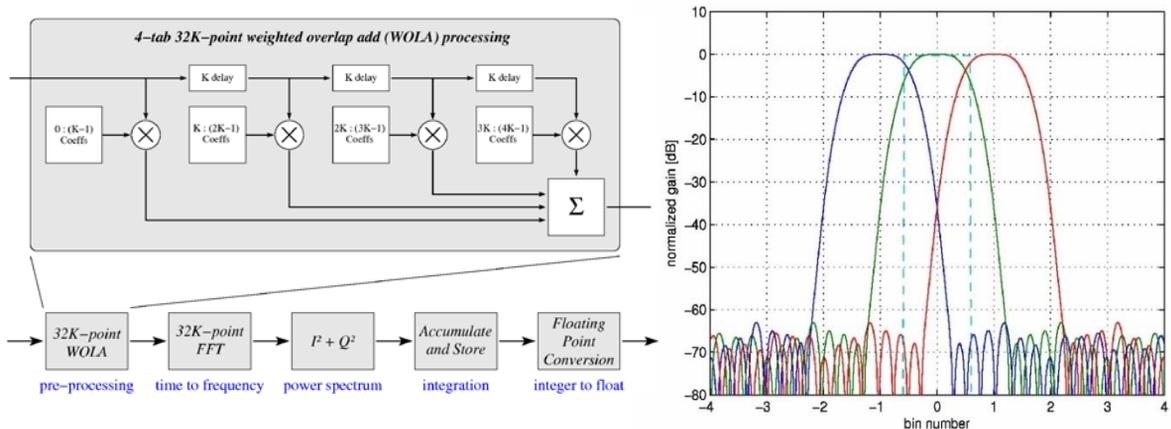
<b>Signal Input</b>	
Full Power Bandwidth (-3 dB)	0.1 GHz to 2.5 GHz (for further details contact RPG)
Input Power	full scale input power: -2 dBm (500 mVpp)
Max. Input Voltage	2 VDC
Impedance	50 Ω
Input Coupling	AC (Balun)
Input Isolation (I/Q) @ 2.6 GHz	> 60 dB (channel-to-channel)
Input Connector	SMA (gold plated)

<b>Digital Conversion</b>	
ADC Type	E2V EV10AQ190
Sample Rate	up to 5 GSPS
ADC Resolution	10 bit (-512 to +511)
ENOB, full bandwidth	7.6 @ 620 MHz 7.2 @ 1200 MHz
SFDR (typical)	>57 dBc @ 620 MHz >55 dBc @ 1200 MHz
Differential Nonlinearity (typ.)	0.3 LSB
Integral Nonlinearity (typ.)	0.8 LSB
<b>Reference Frequency Input (FFTS Controller)</b>	
Ext. Clock/Ref. Threshold	800 mVpp
Maximum Input Voltage	3.0 Vpp
Reference Frequency Range	5 to 250MHz (5MHz step size, programmable)
Input Connector	SMA (gold plated)
<b>Time Base</b>	
Clock Accuracy	50ppm (XFFTS Controller)
Sampling Jitter	< 500fs RMS (10 $\mu$ s record length)
<b>On-Board GPS/IRIG-B Time Decoder</b>	
Standard	IRIG-B 12x, 1kHz, AM modulated
Accuracy (decoding)	< 50 $\mu$ s
<b>On-Board Ethernet Interface</b>	
Standard	IEEE 802.12 (100MBit/s)
Data Rate	80 Mbit/s, sustained

## On-Board Data Processing Unit (DPU)

FPGA (main DPU)	XILINX Virtex-6 XC6VLX 240T
FPGA (Ethernet, etc.)	XILINX Spartan-3 XC3S 1000

### FPGA signal processing pipeline

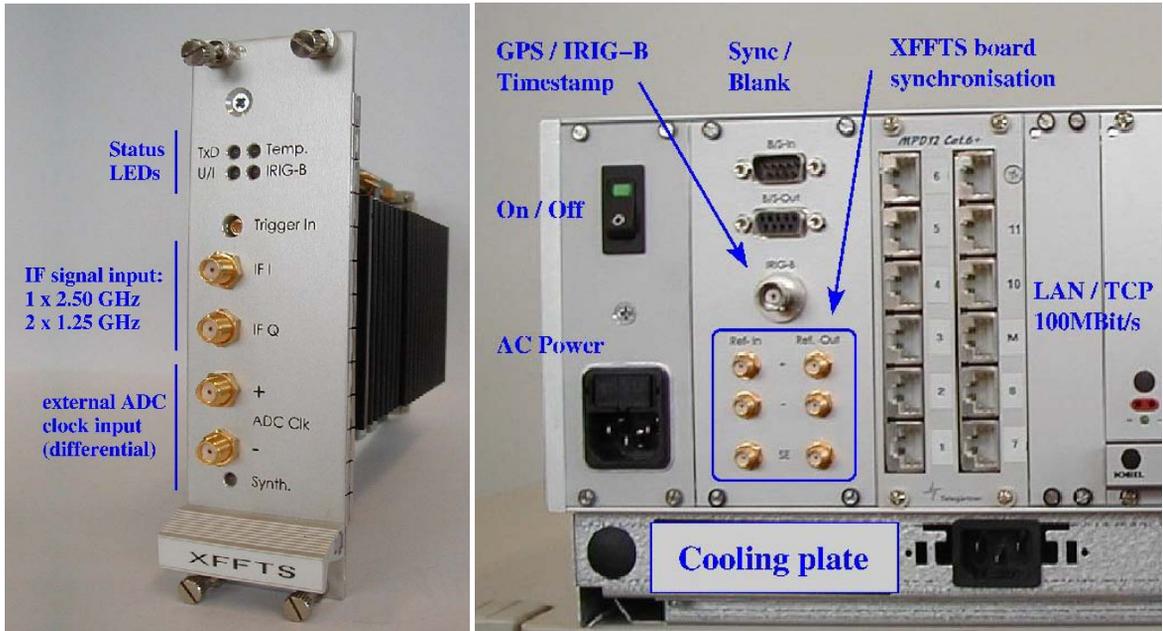


*Left:* Block diagram of the 4-tap polyphase signal processing pipeline implemented in the XFFTS. *Right:* Frequency response of the optimized FFT signal processing pipeline. The diagram shows three adjacent frequency bins in logarithmic scale. The dashed lines illustrate the equivalent noise bandwidth (ENBW) for the corresponding spectral line.

(B. Klein, et al., 2008, 19<sup>th</sup> ISSTT, Groningen, B. Klein, et al., 2009, 20<sup>th</sup> ISSTT, Charlottesville, USA)

Signal Processing / Algorithm	polyphase filter bank (FFT)
Bandwidth (BW)	2.5 GHz (default)
Spectral Channels	32768 (32K) @ 2.5 GHz BW
Channel Spacing	76.3 kHz @ 2.5GHz BW
Resolution (ENBW)	88.5 kHz @ 2.5GHz BW
Internal FPGA Signal Processing	72 bit integer
Processing Output	32-bit single precision (float, IEEE-754)
Spectral Dump Time	max. 5s min. 20ms @ 32k spectral channels

**XFFTS Connectivity:**



PC System Requirements	
Processor (CPU)	Pentium 4 (2GHz or higher) Dual Core CPU recommended
Memory	1 GB RAM (more recommended when working with several XFFTS boards)
Operating System	Linux (Kernel 2.6)
Hard Drive Space	min. 300 MB
<b>Ethernet Switch</b>	A managed Ethernet switch capable of buffering data for each Ethernet port is recommended.

<b>General Data</b>	
<b>Environmental conditions</b>	(indoor use only)
Temperature	
Operating temperature range	0 C to 40 C
Storage Temperature	-30 C to 60 C
Operation Altitude	3000 m (contact RPG for further details)
Required Airflow	>2 m/s
Relative humidity	5-90% (non condensing)
<b>Power supply</b>	
AC Supply	108 VAC to 120 VAC & 216 VAC to 240 VAC 50 Hz to 60 Hz (auto adjust)
Power Consumption	max. 200 W (depending on FPGA core version and operation mode); 4 internal power supplies 5VDC/20A
Dimensions (w x h x d)	480 x 135 x 485 mm 19" crate, 3 units height standard crate, rack mount
Weight	max. 13 kg