Radiometer Physics GmbH

Product Data Sheet

RPG –FFTS

Fast Fourier Transform Spectrometer

Technical Specification

19" FFTS crate equiped with 8 FFTS boards and one FFTS controller (Master)

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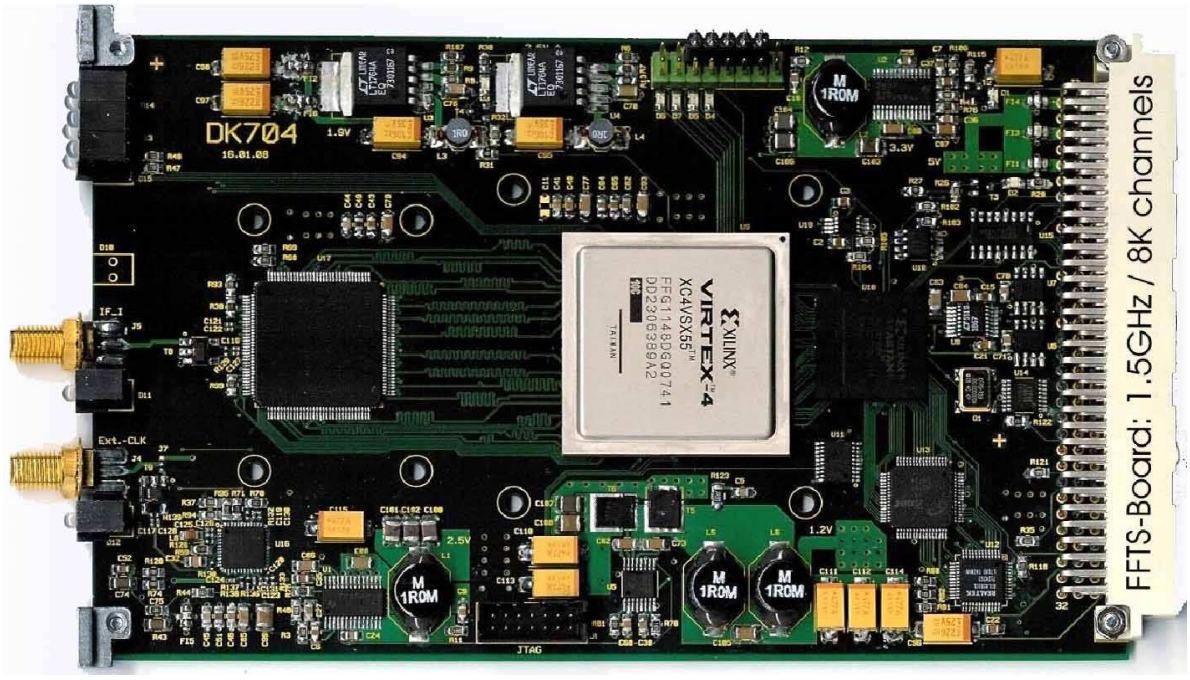
Fast Fourier Transform Spectrometer

The RPG Fast Fourier Transform Spectrometer (FFTS) is optimized for a wide range of radio astronomical applications. The new digitizer and analyzer boards make use of the latest versions of GHz analog-to-digital converters (ADC) and the most complex field programmable gate array chips (FPGA) commercially available today. These state-of-the-art chips made it possible to build a digital spectrometer with instantaneous bandwidth of 1.5GHz and 8192 (8K) spectral channels.

The FFTS is capable of digitizing a baseband mixed intermediate frequency (IF) signal of a heterodyne receiver and transforming this digital data stream into a power spectrum in real time.



Digitizer- / Analyzer Board (FFTS-Board)

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Each FFTS-board operates from a single 5 Volt source and dissipates less than 20 Watt, depending on the actual configuration in terms of bandwidth and number of spectral channels. Precise time stamping of the processed spectra is realized by an on-board GPS/IRIG-B time decoder. Furthermore, the 10-layer boards include a programmable ADC clock synthesizer for a wide range of configurations (bandwidth: 0.1 – 1.5 GHz), making the spectrometer flexible for different observation requirements
The FFTS-boards include a standard 100 MBit/s Ethernet interface, which simplifies the combination of many boards into an Array-FFTS (A-FFTS), simply by integration of a common Ethernet switch. Up to eight FFTS-boards can be housed in one FFTS-crate together with power supplies (4 × 5 Volt / 20 Amperes) and one FFTS-controller (MASTER).

FFTS Master Front Panel

The FFTS-controller manages the synchronization: Reference clock for the on-board ADC synthesizer or the GPS/IRIG-B timing information. In addition, the FFTS-controller displays house-keeping information on a four line LCD, like board IP numbers, temperatures of the ADC and FPGA chips as well as the power level of the IF inputs.

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TECHNICAL DATA

Signal Input	
Full Power Bandwidth	0.1 GHz to 1.5 GHz (for further details contact RPG)
Input Power	full scale input power: 0dBm (630mVpp)
Max. Input Voltage	±1 VDC
Impedance	50 Ω
Input Coupling	AC (Balun)
Input Connector	SMA (gold plated)
Digital Conversion	
ADC Type	National Semiconductors ADC083000
Sample Rate	(2x) 1.45 to 1.8 GHz
ADC Resolution	8 bit (-127 to +128)
Effective Bits (typical)	7.4 @ 248MHz 6.5 @1 498MHz
SFDR (typical)	>55dB @ 248MHz >43dB @ 1498MHz
Differential Nonlinearity	±0.25 LSB
Integral Nonlinearity	±0.35 LSB
Reference Frequency Input (FFTS Controller)	
Ext. Clock/Ref. Threshold	800 mVpp
Maximum Input Voltage	3.0 Vpp
Reference Frequency Range	5 to 250MHz (5MHz step size, programmable)
Input Connector	SMA (gold plated)

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Time Base	
Clock Accuracy	±50ppm (FFTS Controller)
Sampling Jitter	< 500fs RMS (10µs record length)
On-Board GPS/IRIG-B Time Decoder	
Standard	IRIG-B 12x, 1kHz, AM modulated
Accuracy (decoding)	< 50µs
On-Board Ethernet Interface	
Standard	IEEE 802.12 (100MBit/s)
Data Rate	20 Mbit/s, sustained
On-Board Data Processing Unit (DPU)	
FPGA (main DPU)	XILINX Virtex4 SX55, speed grade: 10
FPGA (Ethernet, etc.)	XILINX Spartan XC3S 1000, speed grade: 4

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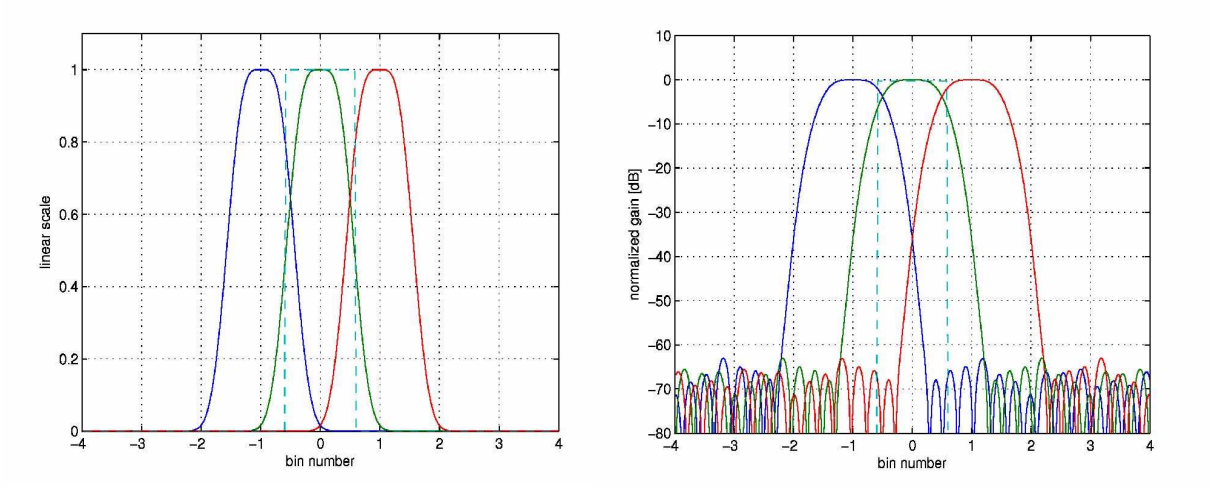
FPGA signal processing /FFT pipeline



Frequency response of the optimized FFT signal processing pipeline. The diagrams shows three adjacent frequency bins. The dashed lines illustrate the equivalent noise bandwidth (ENBW) for the corresponding spectral line. Left: linear scale ; Right: logarithmic scale (B. Klein, et al., 2008, 19th ISSTT, Groningen)

Signal Processing / Algorithm	polyphase filter banf (FFT)
Bandwidth (BW)	1.5GHz (default); max. 1.8GHz
Spectral Channels	8192 (8K) @1.5GHz BW
Channel Spacing	183kHz @1.5GHz BW
Resolution (ENBW)	212kHz @1.5GHz BW
Processing Output	32-bit single precision (float, IEEE-754)
Spectral Dump Time	max. 5s min. 20ms @8k channels min. 5ms @2K channels

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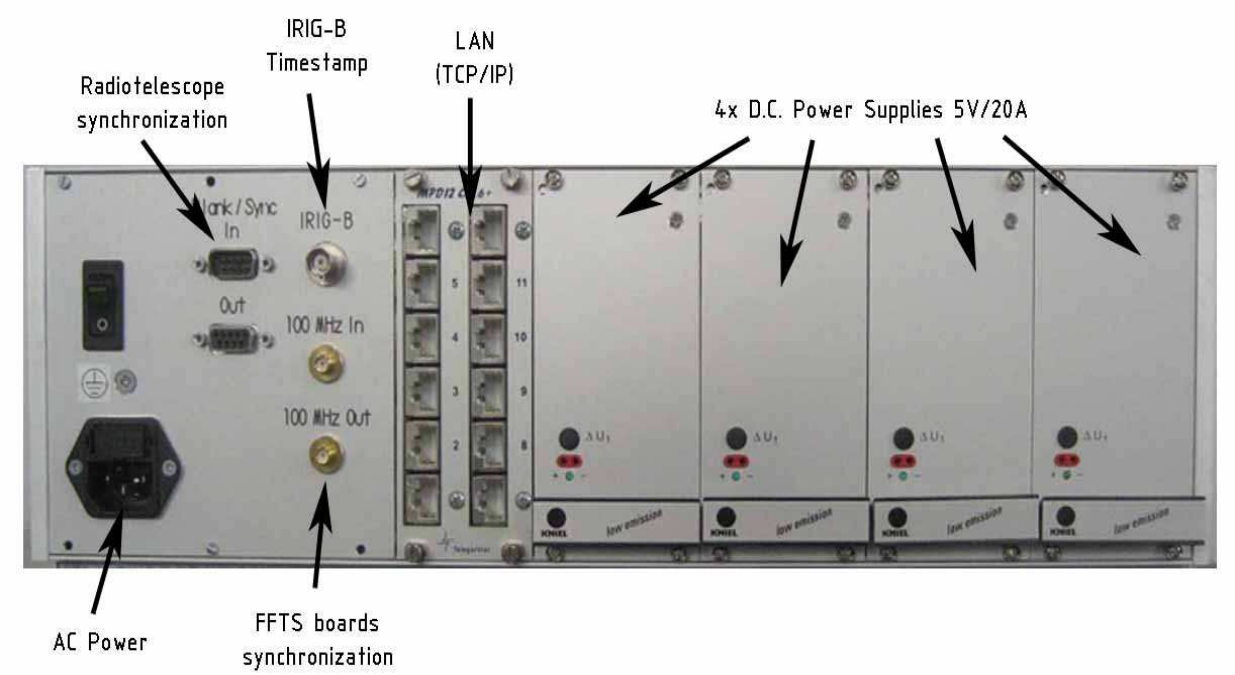
FFTS Crate Rear Panel:



PC System Requirements	
Processor (CPU)	Pentium 4 (2GHz or higher) Dual Core CPU recommended
Memory	1GB RAM (more recommended when working with several FFTS boards)
Operating System	Linux (Kernel 2.6)
Hard Drive Space	min. 200MB
Ethernet Switch	A managed or unmanaged Ethernet switch capable of buffering data for each Ethernet port is recommended

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General Data	
Environmental conditions	(indoor use only)
Temperature	
Operating temperature range	0°C to 40°C
Storage Temperature	-30°C to 60°C
Operation Altitude	3000 m (contact RPG for further details)
Required Airflow	>2 m/s
Relative humdity	5-90% (non condensing)
Power supply	
AC supply	108VAC to 120VAC & 216VAC to 240VAC 50Hz to 60Hz (auto adjust)
Power consumption	max. 200W (depending on FPGA core version and operation mode); 4 internal power supplies 5VDC/20A
Dimensions (wxhxd)	480 x 135 x 485mm 19" crate, 3 units height standard crate, rack mount
Weight	max. 13kg

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